Application Note 48

Implementing the RC5035 and RC5036 DC-DC Converters on Motherboard Designs

Introduction

State-of-the-art microprocessors must integrate an increasing number of functions and provide the flexibility to perform the complex tasks required by today's demanding applications. For this reason, Intel's Pentium® microprocessor architecture has replaced the aging X86 architecture as the computer applications evolve towards multimedia and the Internet.

To support sophisticated multimedia and internet applications, microprocessors integrate a large numbers of transistors onto a single chip. Pentium chips, for example, integrate well over 5 million transistors on a single piece of silicon. To integrate so many transistors onto a small area of silicon, the physical dimensions of each transistor have been reduced to the sub-micron region. As a result of each geometry reduction, the corresponding operational voltage for each transistor has also been reduced. The majority of the logic, control, and memory chips now operate using a 3.3V supply, compared to 5V only 5 years ago. The core logic of the new higher speed Pentium CPUs use under 3.3V. The lower voltage used by the core logic increases the average current required in systems using state-of-the-art microprocessors (see Table 1).

Lower voltages and higher currents have created the demand for fast, flexible, and efficient power supplies. These supplies must be capable of handling 3.3V for the I/O portion of the CPU, and even the lower voltages for the core logic.

Because of the increasing electrical requirements of these CPUs, motherboard designers cannot simply use linear regulators as power supply controllers. To provide a solution to this problem, Raytheon Electronics has developed a series of DC-DC converters. This document describes an efficient dual power supply system for Intel's P55C and AMD's K6 microprocessors using Raytheon's RC5035 and RC5036 Dual Adjustable Voltage Regulators.

P55C and K6 Processor Overview

The P55C and K6 are the third generation of Pentium class microprocessors. They have many feature enhancements for higher performance and are pin compatible with the older Pentium processors. For motherboard designers, the most significant difference between these and older generation processors is the requirement for a dual power supply.

Table 1. CPU Voltage/Current Requirements

Processor	Voltage Required	Description	Current Required
P54	STD 3.3V[1] (3.135 – 3.60V) VRE 3.5V (3.4V – 3.6V)	Core & I/O 512k SRAM Chipset Total	5A 1A 1A 7A
Cyrix 6x86	3.3V (3.15V – 3.60V)	Core & I/O 512k SRAM Chipset Total	7.2A 1A 1A 9.2A
P55C	2.8V±100mv	Core	5.7A
	STD 3.3V (3.135V – 3.60V)	I/O 512k SRAM Chipset Total	0.4A 1A 1A 2.4A
AMD K6	2.9V ±5%/3.2V ±100mV	Core	9.5A
	3.3V (3.135–3.60V)	I/O 512K SRAM Chipset	3A

Note:

1. P54 voltage requirements depend upon CPU type.

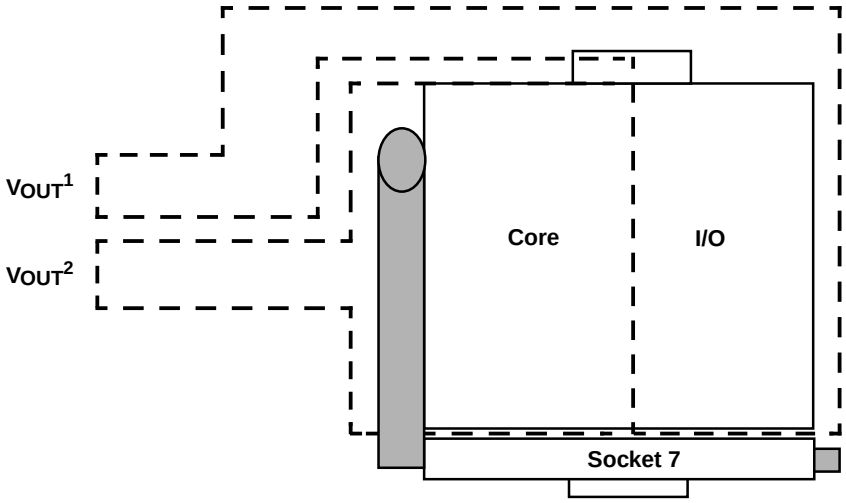


Figure 1. Dual Power Plane with Socket 7 for P55C

The P55C and K6 power supplies are divided in two sections. One is the 3.3V supply that powers the I/O circuitry. The other power supply provides a lower voltage to the CPU core circuitry, typically between 2.5V and 2.9V. As a result of this duality, the motherboard for P55C and K6 requires a dual power plane system as shown in Figure 1.

The P55C and K6 use the VCC2DET pin (as defined on Socket 7) to adjust the voltage of the core power plane to the correct voltage, depending on the CPU installed in the socket. The P55C or K6 force the VCC2DET pin LOW causing the on-board regulator to provide the lower voltage for the core power plane.

P54/P55/K6 Flexible Motherboard

A flexible motherboard allows for a variety of processors to be supported on a single motherboard design, and it can include an auto-configurable regulator circuit. An auto-configurable flexible motherboard must support the 3.3V Standard Range, the VRE s-specification*, the P55C, the K6, and the Pentium OverDrive processors without external jumpers. Figure 2 shows how the RC5035 and RC5036 can implement an auto-configurable voltage regulator system for various CPUs.

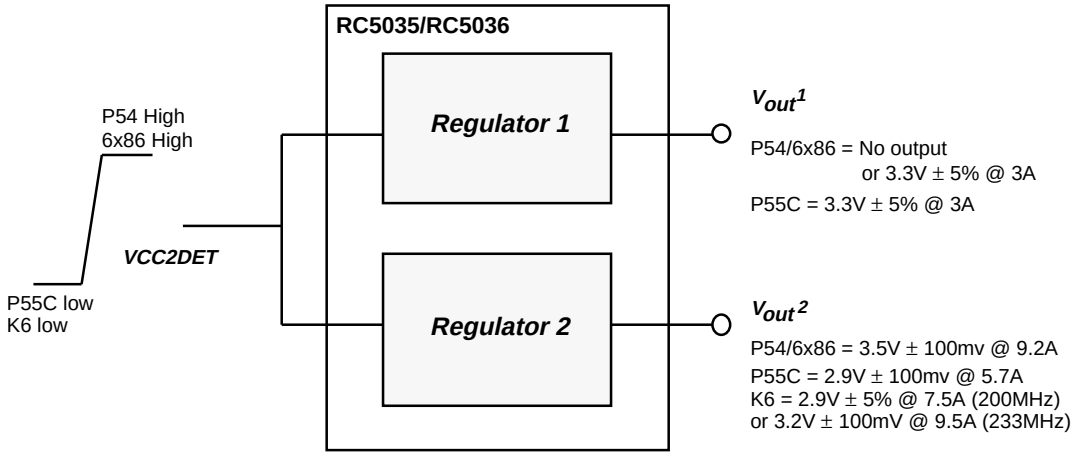


Figure 2. P54/P55 Auto-Configurable Regulator

Implementation Guidelines for 3.3V Pentium Processors with VR/VRE Specifications, Dec. 1994

On P54 Pentium processors and OverDrive processors, the VCC2DET pin is an internal No Connect. It can therefore be set to a high level by an external pull-up resistor. On the P55C and K6, this pin is connected to ground. For the 3.3V and VRE s-specification processors, the switching and the linear regulator portions of the RC5035 and the RC5036 can be driven to 3.3V or 3.5V in the current sharing configuration. Alternatively, the linear regulator can be disabled while the switch-mode regulator supplies the entire current load to the processor.

RC5036 Dual Adjustable Regulator

Description

The RC5036 combines a highly efficient switch-mode DC-DC converter and a precision linear regulator in a single 16 lead SOIC package. With the appropriate external components, this converter can be configured to meet the P54/P55/K6 flexible motherboard requirements. The RC5036 contains the complete control logic for utilizing the VCC2DET pin of the P55C and K6 (see Figure 3). This control function allows the RC5036 to automatically configure a system between the 2.xV core logic voltage for the P55C and K6, and the 3.5V VRE s-specification voltage for the P54.

Functional Description

This section describes the functions of the various internal components of the RC5036.

Main Control Loop

The RC5036 contains a precision trimmed zero TC reference, a constant-on-time architecture controller, a high current output driver, and a low offset operational amplifier. Figure 3 shows how the RC5036 uses external components to form an adjustable dual power supply.

The main control loop for the switch-mode converter consists of a pair of signal conditioning amplifiers. These amplifiers acquire voltage and current information from the regulator output, compare the information against the precision reference, and present error signals to the input of the constant-on-time oscillator. The current feedback controlling signals derive from the voltage developed across the sense resistor that feeds into the IFBH and IFBL inputs to the RC5036. The voltage feedback signal is sent back from the output through a voltage divider to the FBSW pin of the RC5036 to compare against the precision reference. The error signals from both the current feedback loop and the voltage feedback loop are summed together and used to control the off-time portion of the oscillator. The current feedback error signal is also used to provide short circuit protection for the RC5036.

Linear Operational Amplifier

The low-offset operational amplifier is configured to be the controlling element in a precision linear regulator. From Figure 3, the operational amplifier is used to compare the divided output of the linear regulator to the precision reference. The error signal can then be used to control a power NPN transistor.

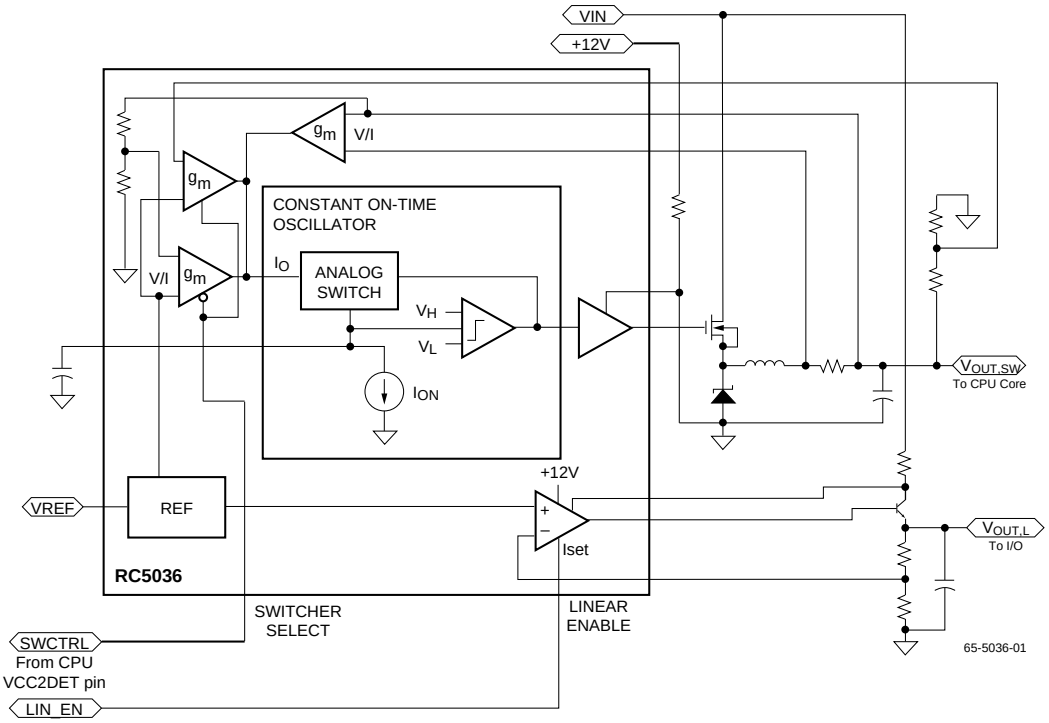


Figure 3. RC5036 Block Diagram

High Current Output Drivers

The RC5036 high current output driver contains high speed bipolar power transistors configured in a push-pull configuration. The output driver can source 1A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The SDRV driver on the RC5036 has a separate power supply, VCCP, which can be obtained from an external 12V source as shown in Figure 5.

Internal Reference

The reference in the RC5036 is a precision band-gap type reference set to 1.5V. Its temperature coefficient is trimmed to provide a near zero TC. For a guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Over-Voltage Protection

The RC5036 constantly monitors of the output voltage for over-voltage protection. If the voltage at the VFBL pin on the RC5036 exceed 20% of the selected program voltage, an over-voltage condition is assumed to exist and the chip shuts down the output drive signals to the power FETs.

Oscillator

The RC5036 constant-on-time oscillator includes a comparator, an external capacitor, a fixed current source, a variable current source, and an analog switch that selects between two threshold voltages for the comparator. The external capacitor is alternately charged and discharged through the enabling and disabling of the fixed current source. The variable current source is controlled from the error inputs that are received from the current and voltage feedback signals. The oscillator off-time is controlled by the amount of available current from the variable current source to charge the external capacitor to the high threshold level of the comparator. The on-time is set by the constant current source that discharges the external capacitor voltage to the lower comparator threshold.

RC5035 Dual Regulator

As can be seen by comparing Figure 3 and Figure 4, the RC5035 is identical to the RC5036 with the exception of the built in switching function on the RC5036. This function allows the RC5036 to be used in P54/P55C/K6 flexible motherboard designs.

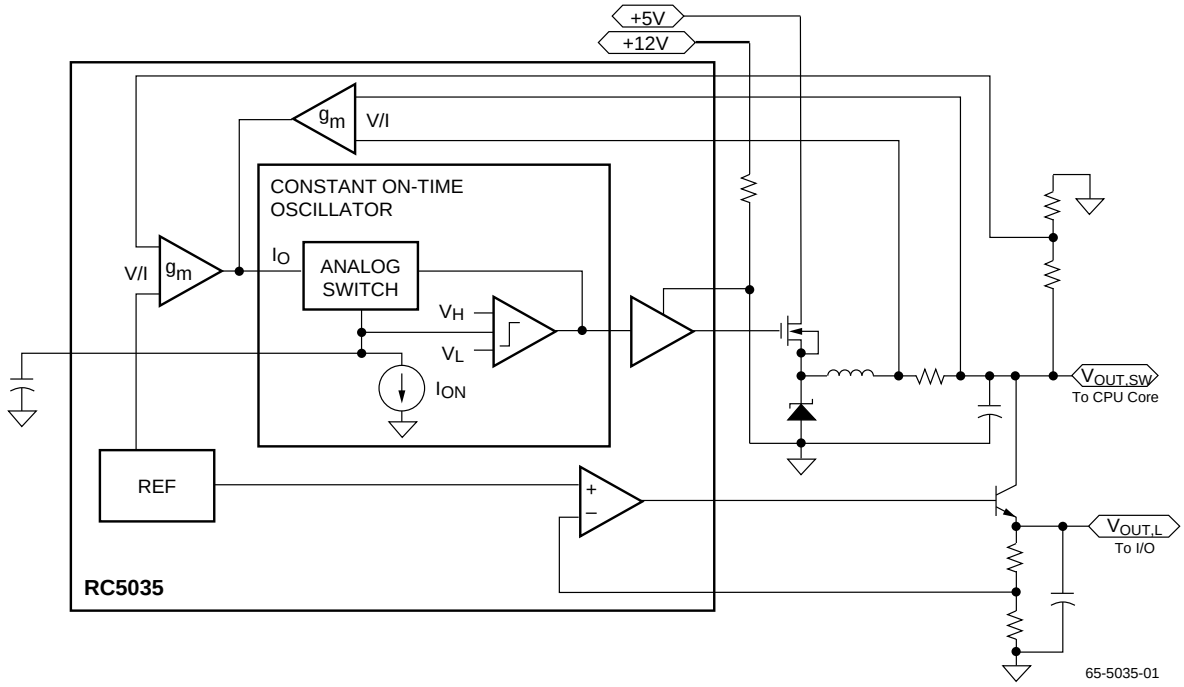


Figure 4. RC5035 Block Diagram

RC5035/RC5036 Evaluation Board

Raytheon Electronics offers an evaluation board to evaluate system level performance of the RC5035 and the RC5036. This board is not intended to be a complete motherboard solution, but rather serves as a guide to the performance of the part using the supplied external components and PCB layout. Appendix B contains the schematic, Bill of Materials, and the complete layout of the evaluation board.

Dual Power Supply Application

Although most of today's desktop computers use multiple output power supplies, lower operating voltages and increased transient response requirements are forcing the move into local power supply systems. Such supplies have inherent advantages of lower parasitic inductance and resistance. The RC5035 and RC5036 address the need for a localized dual power supply for the P55C and K6.

The P55C Pentium processor has increased L1 cache memory over the P54 processor and includes some other refinements in architecture to achieve higher performance levels with multimedia applications. The operating frequency of the core is rated from 150MHz to 200 MHz, with the core supply voltage in the 2.5–2.9V range. For compatibility with previous Pentium processors, the P55C uses an I/O voltage of 3.3V, maintaining compatibility with existing system chipsets and SRAMs. The core current requirement is between 3A and 5A at 2.8V, and the I/O requires 0.4A at 3.3V. The K6 requirements are similar, but the core current requirements are much greater (up to 9.5A).

RC5036 Application

The best application of the RC5036 is to use the switch-mode regulator to provide the 2.xV voltage supply for the core of the P55C and K6. At the same time, the linear regulator can provide the less critical 3.3V power supply for the I/O portion of the design. Figure 5 shows a typical dual power supply configuration.

Using the switch-mode regulator for the core voltage supply has two advantages. First, since the core voltage is dropped below 3V, the high efficiency switch-mode regulator reduces the power dissipation requirements of the power FETs at high currents. Second, the built-in over voltage protection inherent in the switch-mode design protects the CPU core from any voltage related stresses. In addition, the linear regulator can easily handle the 5V to 3.3V conversion at the lower currents without creating a large burden for thermal management.

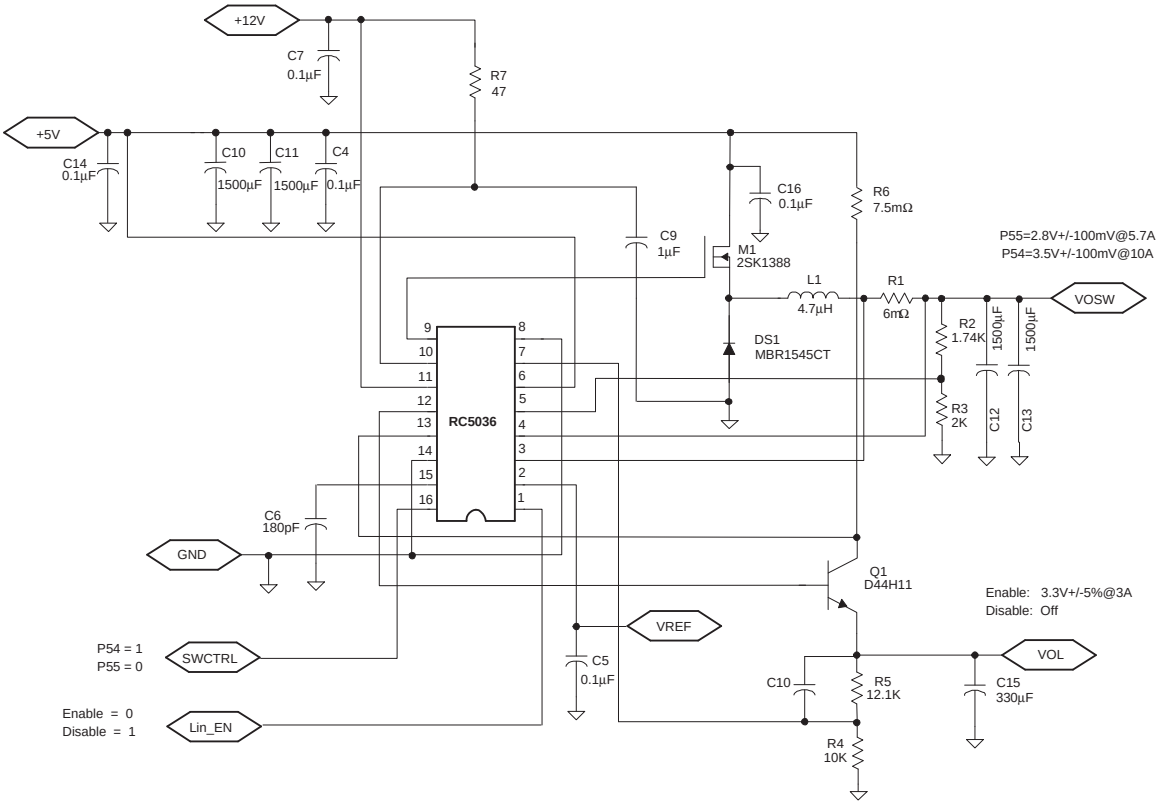


Figure 5. Dual Power Supply for P54/P55C/K6 Flexible Motherboard

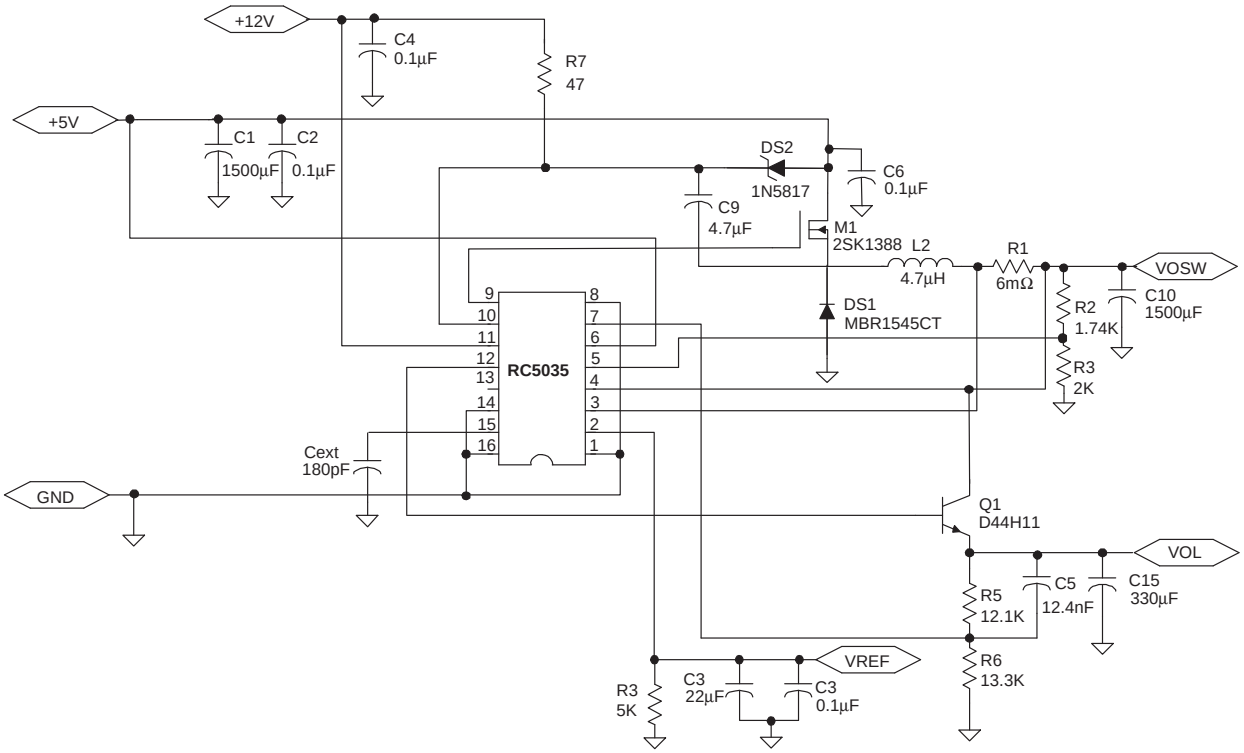


Figure 6. RC5035 with Linear Regulator Slave

RC5035 and RC5036 Application

An application of the RC5035 and the RC5036 is to use the switching regulator as a low-drop-out regulator, as shown in Figure 6. In this application, the switching regulator is used to provide high efficiency conversion from 5V to 3.3V, while the linear regulator is used to drop the 3.3V down to 2.8V (or lower). This approach has the advantage of reducing the power dissipation of the linear regulator FET substantially, to the point that it would not require a heat sink. The disadvantage is that the switching regulator must carry the load current for both the switching output and the linear output.

In the case of P55C, the linear regulator supplies the higher current required by the processor core, rather than the switching regulator in the application of Figure 5. A second disadvantage of this approach is that the switching regulator is required to provide the short circuit current protection for the switcher and for the linear regulator; thus disabling the linear short circuit protection.

However, the linear regulator short circuit protection can be achieved using a differential amplifier with two inputs. The reference input is connected to the chip +5V supply, and the second input is taken from the VSC2 pin. If the input to the power transistor for the linear regulator comes from any supply other than the +5V, the linear short circuit protection function cannot be used.

Figure 7 shows an implementation where the regulator is a single switch-mode regulator operating at 3.3V or 3.5V, but when it detects the VCC2DET in the LOW state, the chip implements a dual supply regulator to address the P55C. In this configuration, the design of a flexible motherboard allows for the switch-mode regulator to carry the highest current for the various processors under consideration. In addition, in this configuration the linear regulator should be designed to supply the P55C processor I/O and other peripheral ICs that may powered by 3.3V.

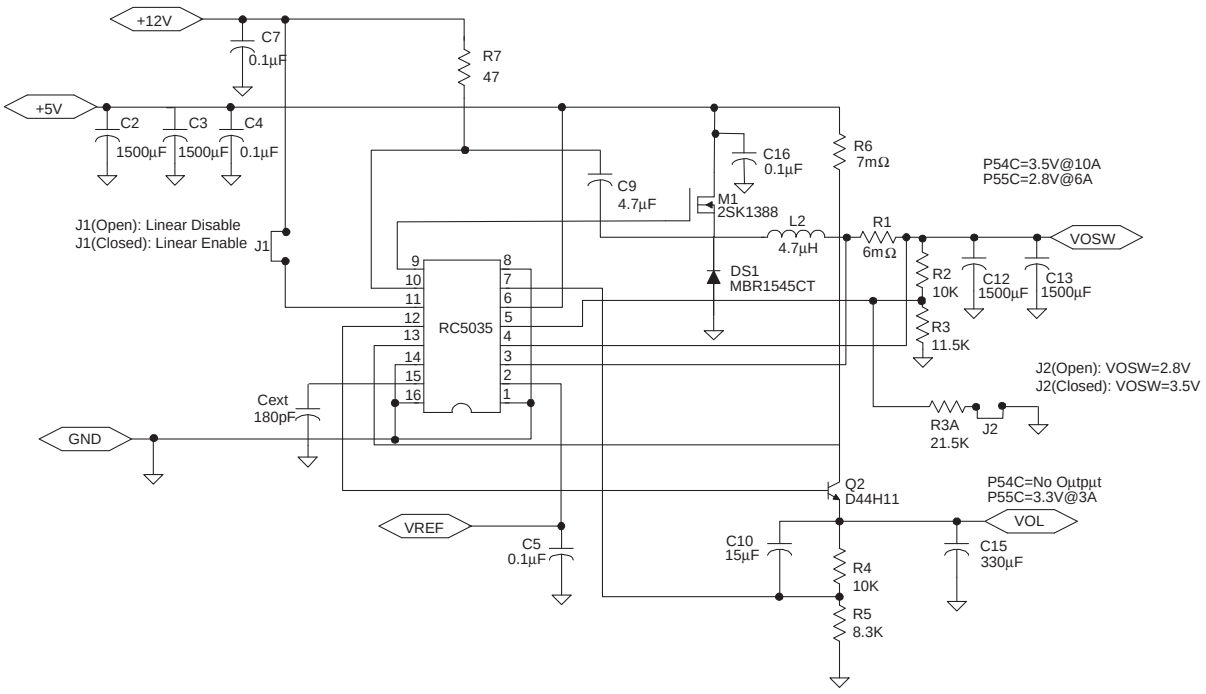


Figure 7. RC5035 Implementation for P54/P55C/K6 Flexible Motherboard

Detailed Design Relationships

Generalized Design Equations

The derivation of the basic step-down buck regulator design equations are the basis for the design relationships for the RC5035 and the RC5036. Figure 8 shows the basic step-down DC-DC converter without a feedback controller.

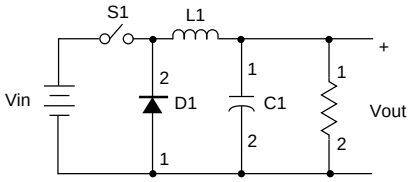


Figure 8. Simplified Step-Down DC-DC Converter

The basic operation is realized in two steps. Step one occurs when switch S1 is closed, providing voltage on the inductor L1. The current flowing through the inductor is calculated from the following relationship (assuming an ideal switch):

$$V_{IN} - V_{OUT} = L1\frac{(I_{PK} - I_{MIN})}{T_{ON}}$$

Step two occurs when switch S1 is open, making diode D1 drive the current through the inductor. The current through the inductor decreases at the following rate:

$$V_D + V_{OUT} = L1\frac{(I_{MIN} - I_{PK})}{T_{OFF}}$$

By rearranging these two equations, we can arrive at the basic relationship for the step-down buck regulator. These equations are valid for the assumption that the regulator is operating in the continuous mode (design equations for a regulator operating in the discontinuous mode are not discussed here).

Figure 9 shows a pictorial representation of the voltage and current relationships described for the step-down regulator.

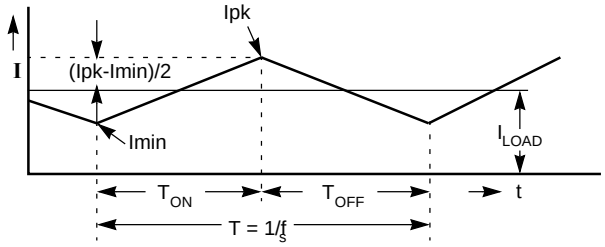


Figure 9. Inductor Current Relative to Period

The Duty Cycle is calculated by:

$$\frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} = \frac{T_{ON}}{T} = \textit{Duty Cycle}$$

where T is the total period of the clock, $T_{ON} + T_{OFF}$, and V_D is the diode forward voltage $V_{SW} = I_O \bullet R_{DS,ON}$.

Specific Design Equations

The above general relationships are the basis for the specific design relationships used for selecting the proper inductance and capacitance for the design under consideration.

Selecting the Inductor

The inductor is one of the most critical components to be selected for a DC-DC converter application. The critical parameters are inductance (L), maximum DC current (I_O), and coil resistance (Rl). The core material is a critical factor for determining the amount of current that the inductor can handle. As with all engineering designs there are trade-offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however, they are expensive and more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance degrades the efficiency of the converter by:

$$P_{LOSS} = I^2 \times R_{DC}$$

where I is the average load current in the inductor and R_{DC} is the DC resistance of the inductor.

The value of the inductor is a function of the switching frequency (T_{ON}) and the maximum inductor current, I_{PK}. The maximum inductor current can be calculated as follows:

$$I_{PK} = I_{MIN} + \left(\frac{V_{IN} - V_{SW} - V_O}{L}\right) T_{ON}$$

Where T_{ON} is the maximum on time of the M1 FET and V_{SW} is the drain-to-source voltage dropped by the FET.

The inductor value can be calculated by:

$$L = \left(\frac{V_{IN} - V_{SW} - V_O}{I_{PK} - I_{MIN}}\right) T_{ON}$$

Current-Sense Resistor

The current sense resistor carries all of the peak current of the inductor. The peak current is larger than the load current. The RC5035 and RC5036 begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage temporarily goes out of regulation. As the voltage across the resistor increases, the top-side FET turns off more and more until the current limit value is reached. Only then can the chip continuously deliver the limit current at a reduced output voltage level.

When designing the external current sense circuitry, pay careful attention to the output limitations during normal operation and during a fault condition. If the short circuit protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. The design equations used to set the short circuit threshold limit are as follows:

$$I_{Inductor} = I_{load} + (I_{PK} - I_{MIN})/2$$

$$I_{SC} = \frac{V_{th}}{R_{SENSE}}, \text{ where: } I_{SC,\,MIN} > I_{PK}$$

Since the value of the sense resistor is generally in the milliohm region, trace resistance can contribute significant errors. Therefore, care should be taken in the layout of the PCB. The traces to the IFBH and IFBL pins of the RC5035 and RC5036 should be Kelvin connected to the pads of the current-sense resistor. To minimize the influence of noise, the two traces should be run next to each other, or an embedded sense resistor can be integrated into the PCB.

The sense resistor value can be approximated by:

$$R_{SENSE} = \frac{V_{th,min}}{I_{PK}} \times (1 - TF) = \frac{V_{th,min}}{0.5 + I_{LOAD,MAX}} \times (1 - TF)$$

Where TF = Tolerance Factor for the sense resistor.

Different types of sense resistors exist. Table 2 describes the tolerance, size, power capability, temperature coefficient, and cost of various types of sense resistors.

Table 2. Comparison of Sense Resistors

	Motherboard Trace Resistor	Discrete Iron Alloy Resistor (IRC)	Discrete Metal Strip Surface Mount Resistor (Dale)	Discrete MnCu Alloy Wire Resistor
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.200"	0.25" x 0.125" x 0.025"	0.200" x 0.04" x 0.160"
Power capability	> 50A/in	1 watt (3 and 5 watts available)	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm
Cost@10,000 piece quantity	Low; included in motherboard	$0.31	$0.47	$0.09

The following equations are based on the Tolerance Factor in Table 2.

For an embedded PC trace resistor:

$$R_{SENSE} = \frac{V_{th,min}}{0.5 + I_{LOAD,MAX}} \times (1 - TF) = \frac{80mV}{0.5A + 10A} \times (1 - 29\%) = 5.4m\Omega$$

For a discrete resistor:

$$R_{SENSE} = \frac{V_{th,min}}{0.5 + I_{LOAD,MAX}} \times (1 - TF) = \frac{80mV}{0.5A + 10A} \times (1 - 5\%) = 7.2m\Omega$$

Table 3 lists recommended values for sense resistors for various load currents using an embedded PC trace resistor or a discrete resistor.

Table 3. R_{sense} for Various Load Current

$I_{LOAD,MAX}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
5	10.3	13.8
6	8.7	11.7
7	7.6	10.1
8	6.7	8.9
9	6.0	8.0
10	5.4	7.2

Feedback Voltage Divider

The RC5035 and RC5036 precision reference is trimmed to 1.5V nominally so that the system designer has control over choosing the output voltage for each regulator, from 1.5V to 3.6V. Hence, the design procedure includes the setting of the feedback resistors. These resistors should be 0.1% accurate resistors to obtain the best accuracy results. The value of the resistors is an important consideration, because choosing the total resistance of the divider network incorrectly can negate the effect of using 0.1% resistors. The following equations relate the output voltage to the reference voltage.

Switching Regulator:

$$V_{OUT} = V_{REF}\left(\frac{R2 + R3}{R3}\right)$$

Linear Regulator:

$$V_{OUT} = V_{REF}\left(\frac{R4 + R5}{R4}\right)$$

Where:
R2 > 1.5KΩ and (R2 + R3) ≤ 25KΩ
R4 > 1.5KΩ and (R4 + R5) ≤ 25KΩ.

Since the voltage reference for the RC5035 and RC5036 is 1.5V, the linear regulator equation becomes:

$$V_{OUT} = 1.5V\left(\frac{R4 + R5}{R4}\right)$$

Assuming that R4 is the resistor connected between the feedback pin of the regulator chip and ground, and setting V_{OUT} to 3.3V, then:

$$R5 = R4\left(\frac{3.3 - 1.5}{1.5}\right) = 1.2(R4)$$

Thus, if R4 is 50K, then R5 would be 60K.

Since the voltage divider connects to the input of a bipolar operational amplifier inside the DC-DC converter chip, the effect of the input current on the accuracy of the voltage divider network must be evaluated. If the input bias current of the operational amplifier was on the order of 1µA, the effect of the current can be calculated by finding the total bias current required for the divider network.

$$I_{NET} = \frac{3.3V}{50K + 60K} = 30\mu A$$

A 1µA input current yields a 3.3% error in the output voltage due to the input current required for the RC5035 or RC5036 operational amplifier. Hence, the 50K and 60K resistors are not good choices. If the resistors are reduced by a factor of 10, to 5K and 6K, then the 1µA input current produces an acceptable 0.3% error.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5035 and RC5036. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the FET. Low ESR (Equivalent Series Resistance) capacitors are best suited for the application described in this document. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by large trace lengths.

The ESR (defined as the real part of the resonant impedance of the capacitor) rating of a capacitor is a difficult number to obtain. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data, but a useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

Where DF is the capacitor's dissipation factor, f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. An estimate of the bulk decoupling capacitance required can be obtained using the following equation:

$$C = \frac{I \times \Delta t}{\Delta V - I \times ESR}$$

Where Δt is the period over which the CPU demands current from the capacitors, and ΔV is the maximum allowed voltage change over that period.

Schottky Diode Selection

The circuit in Figure 5 shows a Schottky diode, DS1. This diode should have a low forward voltage drop because it directly affects the regulator efficiency. During the off time of the power FET, M1, the voltage on the inductor drops until the DS1 clamps and conducts full current through the inductor. The power in DS1 ($P_D = V_F \times I_L$) is a direct subtraction from the overall efficiency of the converter. Thus, DS1 should have a low V_F to minimize the power-loss term. A diode selection guide is given in Appendix C.

MOSFET Switches

The MOSFET switch in a RC5035 and RC5036 application circuit is an N-channel logic-level FET. Thus, the switch is fully on when Vgs is 4V. Many manufacturers make logic-level FETs but you should choose the one with the lowest $R_{DS(ON)}$ at the given Imax current level. $R_{DS(ON)}$ enters into the efficiency equation as a power loss. In addition, the efficiency is influenced by the gate charge of the FET and the clock frequency of the DC-DC converter chip. At higher clocking rates the amount of charge needed to be delivered to the FET lowers the overall efficiency. A selection guide for logic-level MOSFETs is given in Appendix C.

Timing Capacitor

To select the appropriate timing capacitor you must consider the design trade-offs between frequency, maximum expected load current, efficiency, and response time. In general, the frequency, response time, and efficiency are inter-related. However, since the RC5035 and RC5036 rely on a constant-on-time control for the PWM function, you should also take into account the maximum load current.

The PWM controller modulates the current switch to provide the correct current ramp on the inductor. The amount of charge and discharge in the inductor determines the average load current at any given time. The RC5035 and RC5036 modulate the current switch by adjusting the off-time in response to the feedback inputs obtained from the regulator output. That is, in response to varying load conditions, the regulator chips adjust the frequency of the oscillator to modulate the off-time of the FET. Thus, for an increasing current load, the RC5035 and RC5036 increase the frequency to release more charge into the inductor (see Figure 10).

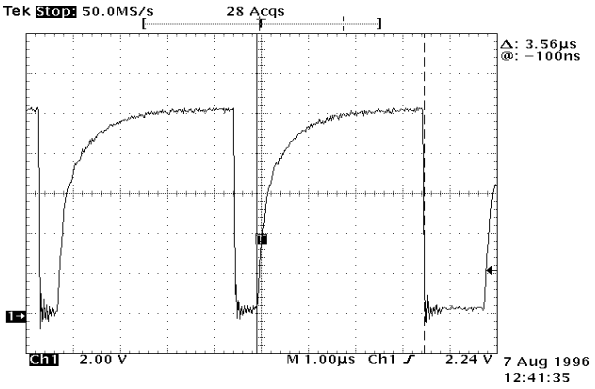


Figure 10. Scope Photo of Pin 9 at a 5Amp Load

Conversely, as the current load is reduced, the RC5035 and RC5036 adjust the oscillator frequency to maximize the FET off-time (see Figure 11). Doing this ultimately places upper and lower limits on the operating frequency of the chip's oscillator.

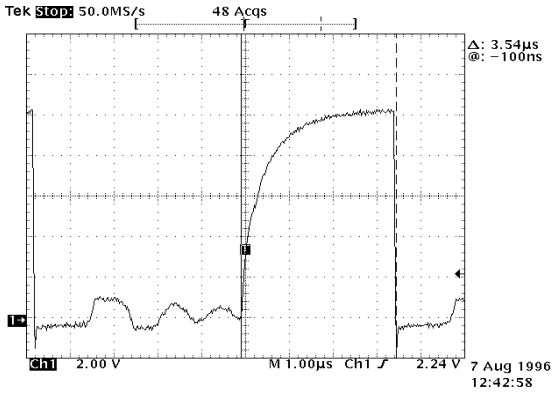


Figure 11. Scope Photo of Pin 9 at a 0.1A Load

Figure 12 shows the relationship between the nominal oscillator frequency and the C_{EXT} capacitance. In general, the lower the oscillator frequency (larger C_{EXT}), the better the overall efficiency of the design, but load regulation and response time are diminished. The higher the oscillator frequency, the better the transient response time and the load regulation. These factors must all be weighed together when deciding the appropriate C_{EXT} capacitor.

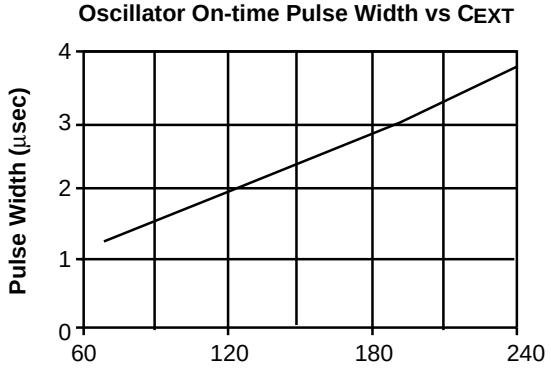


Figure 12. Pulse Width vs. Capacitance

Linear Regulator Design Considerations

The RC5035 and RC5036 linear regulators can be configured in several ways depending upon the application requirements. The most cost effective solution is using an NPN bipolar transistor as the high power pass element. This solution can be used effectively to provide 3.3V from a +5V supply as shown in Figure 5. The considerations when using this approach involve the output current capability of the linear regulator operational amplifier and the thermal dissipation of the 16 lead SOIC package. The bipolar transistor should have a Beta > 80 in order to limit the base current required from the linear operational amplifier. A thermal analysis performed on the application in Figure 5 shows the reasons for the design requirement of a greater than 80 Beta.

For reliability, the junction temperature must not exceed 120°C. Then, the maximum power dissipation allowable for the 16 lead SOIC package can be calculated by:

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\Theta JA}}$$

Assuming that the ambient temperature T_A is 50°C and the thermal resistance of the 16 lead SOIC package is 150°C/W, then the maximum power dissipation for the RC5035 and RC5036 is:

$$P_D = \frac{120 - 50}{150} = 0.466W$$

Using a typical power transistor, the D44H11 for example, the minimum Beta for operation a 3A is approximately 50 at 25°C. This may appear to violate the above requirement of Beta > 80, but further analysis shows that the Beta in the actual application is much higher. Beta increases over temperature; thus, the junction temperature of the power transistor under a 3A load, is:

$$P_D = I \times V_{CE} = 3A \times (5 - 3.3) = 5.1W$$

Using the equation for obtaining the junction temperature, we have:

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\Theta JA}} = 5.1W$$

For a TO-220 package with the appropriate heat sink, the $R_{\Theta JA}$ is about 8°C/W. Assuming that the ambient temperature is 50°C, $T_{J(max)}$ is:

$$P_D \times R_{\Theta JA} + T_A = T_{J(max)} = 5.1W \times 8 + 50 = 90.8°C$$

Thus, the transistor Beta is much higher than the minimum required value. A transistor with a rated Beta minimum of 50 at 25°C should yield a Beta of 80+ under the above ambient conditions.

Now, the RC5035 and RC5036 power dissipation due to the base current required by the NPN transistor can be calculated, with a minimum Beta of 80. At the maximum load of 3A, the base current is 3A/80 = 37.5mA. Since the output of the transistor is 3.3V, the base voltage is one diode drop higher, 3.3V + 0.7V = 4V. Thus, if the RC5035 and RC5036 VCCL supply (the VCC supply for the operational amplifier) is connected to 12V, then the power dissipation of the chip due to the linear regulator is:

$$P_D = (12V - 4V) \times 37.5mA = 0.3W$$

Hence, at the maximum current of 3A, the power dissipation of the RC5035 and RC5036 is within the maximum power allowed at an ambient temperature of 50°C.

Motherboard Design Considerations

Modern high speed computers require careful attention to all aspects of PC board design, both electrical and thermal. In addition, with I/O bus speeds running at 66MHz and power supply currents in the 10 Amp range, each phase of the motherboard design requires careful attention to the parasitic resistance and capacitance on the PCB.

Electrical Design Considerations

A dual power plane design presents a variety of challenges in design, especially because one plane is split to serve both the core voltage and the I/O. Care must be taken to insure that the planes have adequate area for the currents that flow to the CPU. The RC5035 or RC5036 needs to be located fairly close to the CPU in order to reduce the IR drop. And, when designing with a switch-mode regulator, trace lengths to reduce RF noise must be minimized. This is especially true for the high frequencies of the RC5035 and RC5036. Most of the design problems associated with a switch-mode regulator derive from the initial component placement. The following sections should serve as a step-by-step procedure to follow when designing with the RC5035 or RC5036.

Regulator Chip Placement

The RC5035 or RC5036 should be placed as close to the Vcore side of the P55C as possible. Preferably the PC layer that is directly underneath the regulator should be the ground layer to serve as extra isolation from the noisy power planes.

MOSFET Placement

Placement of the power MOSFET is critical in the design of the switch-mode regulator. The FET should be placed so as to minimize the length of the gate drive signal from the RC5035 or RC5036. Excessive lead length on this trace causes high frequency noise from the parasitic inductance and capacitance of the trace. Since the voltage can transition nearly 12V in approximately 100nsec, the resulting ringing and noise is very difficult to suppress. The trace should be routed on one layer only and kept far away from the quiet analog pins of the device: VREF, CEXT, FBSW, IFBH, IFBL, and VFBL (see Figure 13).

Inductor and Schottky Diode Placement

The inductor and fly-back Schottky diode must be placed close to the source of the power MOSFET. Excessive lead length on this trace causes high frequency noise from the parasitic inductance and capacitance of the trace. The node between the inductor and the Schottky diode swings between the drain voltage of the FET and the forward voltage of the diode. It is recommended that this node be converted to a plane if possible. This node is part of the high current path in the design, and as such it is best treated as a plane to minimize parasitic resistance and inductance on that node. Most PC board manufacturers use 1/2 oz. copper on the top and bottom signal layers of the PCB. These layers should not be used to route the high current portions of the regulator design. Since it is more common to use 1 oz. copper on the

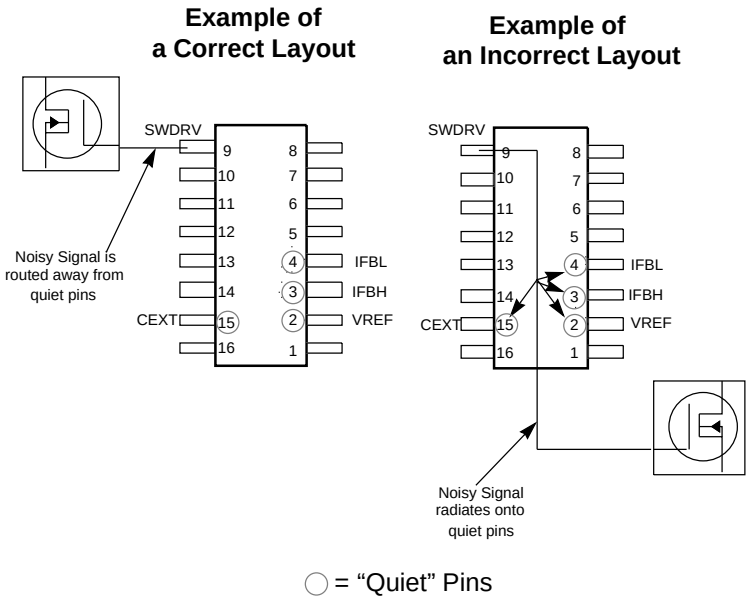


Figure 13. Example of Correct and Incorrect Layout

PCB inner layers, use those layers to route the high current paths in the design.

Capacitor Placement

The correct placement of the low ESR capacitors is key to a successful switch-mode power supply design. Decoupling capacitors must serve two purposes: support the expected transient current of the CPU and provide noise suppression over a wide range of frequencies. To support the expected transient current of the CPU, enough bulk capacitance is required. To provide noise suppression, a variety of capacitor types and capacitances are required.

Low ESR capacitors on the input side (5V) of the FET must be located close to the drain of the power FET; thus, minimizing parasitic inductance and resistance critical in suppressing the ringing and noise on the power supply. Low ESR output capacitors must be placed close to the output sense resistor to provide good decoupling at the voltage sense point.

The impedance on good low ESR capacitors gradually increases as the frequency increases. Thus, for high frequency noise suppression, good quality low inductance ceramic capacitors (usually, 0.1µF surface mount capacitors) should be placed in parallel with low ESR bulk capacitors.

Power and Ground Connections

The connection of the VCCA pin to the 5V power supply plane should be short and bypassed with a 0.1µF capacitor set directly on the pin. The ideal connection is directly to the 5V power plane. Designs that use an input inductor, should connect VCCA to the input of the inductor as shown in Figure 5. A similar arrangement should be made for the VCCL pin that connects to the +12V supply plane. Each ground should have a separate connection to the ground plane.

Embedded Sense Resistor (PC Trace Resistor)

Three major error sources must be considered when laying out embedded sense resistors, described as follows.

Sheet Resistivity

For 1 ounce copper, the thickness variation is typically between 1.15 mil and 1.35 mil. Therefore, the error due to sheet resistivity is (1.35–1.15)/1.25 = 16%.

Mismatch Due to L/W

The percent error in L/W is dictated by the geometry and the power dissipation rating of the sense resistor. The resistor must be able to handle the load current, requiring a minimum width which is calculated by:

$$W = \frac{I_L}{0.05}$$

where W is the minimum width required for proper power dissipation (in mils) and I_L is the load current in Amps.

For example, 10A of load current requires a minimum width of 200 mils which reflects a 1% L/W error.

Thermal Consideration

I^2R power losses result in increased surface temperature of the resistor, thus increasing the value of the resistor. In addition, ambient temperature variations add to the change in resistor value:

$$R = R_{20}[1 + \alpha_{20}(T - 20)]$$

where R_{20} is the resistance at 20°C, α_{20} = 0.00393/ °C, T is the operating temperature, and R is the desired value.

For temperature T = 50°C, the %R change = 12%.

Summary

Table 4 is a summary of the tolerances for the Embedded PC Trace Resistor.

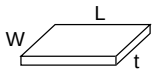
Table 4. PC Trace Resistor Tolerance Summary

Tolerance due to Sheet Resistivity variation	16%
Tolerance due to L/W error	1%
Tolerance due to Temperature Variation	12%
Total Tolerance for PC Trace Resistor	29%

Design Rules for Using an Embedded Resistor

The basic equation for laying out an embedded resistor is:

$$R = \rho \times \frac{L}{W \times t}$$



where ρ is Resistivity (µΩ–mil), L is Length (mils), W is Width (mils), and t is Thickness (mils).

For 1 oz. copper, t = 1.35 mils, ρ = 717.86 µΩ-mil, and 1 L/1 W = 1 Square □.

For example, to layout a 5.3mΩ embedded sense resistor, W = 10/0.05 = 200 mils.

Now, L (mils) = 0.00530*200*1.35/717.86 = 2000 mils, and L/W = 10 □.

Therefore to model 5.30mΩ, one needs W = 200 mils, and L = 2000 mils (see Figure 14).

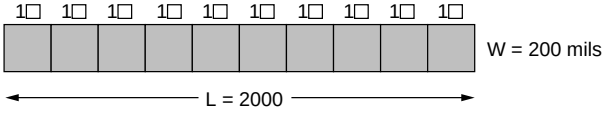


Figure 14. 5.30 mΩ Sense Resistor (10 □)

You can also implement the sense resistor in the following manner. Each corner square is counted as 0.6 square since current flowing through the corner square does not flow uniformly, concentrated towards the inside edge. See Figure 15.

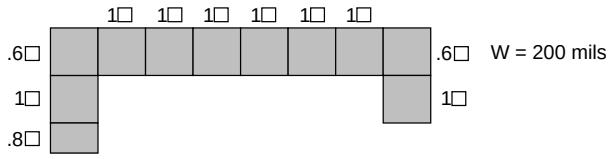


Figure 15. 5.30 mΩ Sense Resistor (10 □)

A Design Example Combining an Embedded Resistor and a Discrete Resistor

For a low cost implementation, the embedded PC trace resistor is more effective. However, the wide tolerance (±29%) of this resistor presents a challenge. The following design example provides a flexible solution for wide tolerances.

When using Raytheon's RC5036 demonstration board (Figure 16), you have the option to choose an embedded or a discrete MnCu sense resistor. To use the discrete sense resistor, populate R21 with a shorting bar (zero Ohm resistor) for proper Kelvin connection and add the MnCu sense resistor. To use the embedded sense resistor, populate R22 with a shorting bar for Kelvin connection. The embedded sense resistor allows you to choose a plus or a minus delta resistance tap to offset any changes that may be attributed to junction temperature increments, or due to layout inaccuracies. That is, by running a thick jumper between the Vout plane and the center tap gives approximately 6mΩ. Similarly, the left or the right tap give approximately 6.7mΩ or 5.3mΩ as the sense resistor value.

Thermal Design Considerations

Good thermal management is also critical in the design of high current regulators. System reliability is degraded if component temperatures become excessive. Use the following sections as a reference in designing for good thermal management.

MOSFET Temperature

The power dissipation of the FET can be calculated by:

$$P_D = \frac{T_{J(max)} - T_A}{\Theta_{JA}}$$

For the Fuji 2SK1388 FET, Θ_{JA} is 75°C/W. For reliability the junction temperature of the FET should not exceed 120°C. Assuming that the ambient temperature is 25°C, then the power dissipation is:

$$P_D = \frac{120 - 25}{75} = 1.267W$$

By placing the FET on the PC board and utilizing the power plane as a heatsink, the Θ_{JA} can be reduced by a factor that corresponds to the surface area. For a 1 inch square area, the Θ_{JA} drops to approximately 40°C/W, so that,

$$P_D = \frac{120 - 25}{40} = 2.37W$$

The power that the FET dissipates at the rated 8A load is calculated as follows:

$$P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$$

$$P = (64)(.037)\frac{3.3 + 0.4}{5 + 0.4 - 0.2} = 1.68W$$

Since the power at 8A is within the thermal guideline, a heat sink is not required other than the PCB. When the current is 11A, a similar calculation can be performed for power dissipation:

$$P = (121)(.037)\frac{3.3 + 0.4}{5 + 0.4 - 0.2} = 3.18W$$

Clearly this power level exceeds the thermal guideline set above. For a 120°C maximum junction temperature, a single FET requires a heatsink or more surface area in order to reduce the Θ_{JA}.

Parallel FETs

An alternate method for reducing the power dissipation on the FET is to connect two power MOSFETs in parallel. In this case, the FETs share the load current and can eliminate the need for a heatsink. Be careful when designing with parallel FETs: make sure that the high current paths to the drain and from the source are equal, and that the gate drive signals to the FETs have the same propagation delay. These considerations are critical for the FETs to properly share the load current. The following is an example of the thermal improvement with parallel MOSFETs.

If two FETs are in parallel, the system effectively drops the current through each FET. The power dissipation of each FET is given by:

$$P = (5.5)(.037)\frac{3.3 + 0.4}{5 + 0.4 - 0.2} = 0.79W$$

This magnitude of improvement compounds upon itself because as the power dissipation of the FET drops, so does the $R_{DS(ON)}$. This improvement manifests itself in higher overall conversion efficiency for the regulator.

Schottky Diode

A similar analysis can be made for the fly-back Schottky diode. In the non-synchronous design, the fly-back diode carries the full current of the output load when the power MOSFET is turned off. Thus, a thermal analysis is in order

for this component. The power in the diode is a direct function of the forward voltage at the rated load current during the off time of the FET. The following equation can be used to estimate the diode power:

$$P_D = (I_{OUT})(V_F)T_{OFF}$$

Using the example of a regulator supplying 11A to the load once more, the power in a Motorola MBR2030CTL Power Rectifier can be calculated. From the Motorola data book, the Vf of the diode at 11A is 0.5V. If the regulator is performing a 5V to 3.3V conversion, then the off time is (1 - Duty Cycle). For 5V to 3.3V, the duty cycle is approximately 0.71.

Since this device is in a TO-220 package, a comparison can be made between its thermal resistance and the calculation above. The maximum power for a free standing TO-220 device = 1.267W. Since the calculated number is higher, a heatsink must be added, or the package should be mounted onto the PCB so that it serves as heatsink.

Characterizing and Debugging the Design

This section provides a systematic approach to debugging and characterizing an initial RC5035/RC5036 regulator design. If all of the above mentioned design guidelines have been followed, then the debugging of the first design is straight forward. A discussion of the equipment required for testing the design, the methodology for debugging the design, and what is required to perform a thorough characterization is presented is this section.

Equipment Required

The following are the minimum equipment required for testing the performance of the regulator:

- 41/2 Digit DVM
- Analog or Digital scope (100Mhz BW)
- Current Load (Active)
- PC “Silver Box” Power Supply

The following additional equipment can be useful for characterizing the performance of the regulator:

- Current Probe
- Intel Transient Tester

Debugging the First Design

Testing the switching regulator design is discussed first because regulator encompasses more areas of concern than does the linear regulator. In debugging the switching regulator design, a methodology must be followed. The cost of the CPU is at least 2–3 times the cost of the PC motherboard, so the power supply to the CPU must work properly to avoid any damage. Hence, a thorough evaluation of the power supply is required prior to plugging the CPU into the socket on the motherboard.

Step 1: Initial Measurements

The initial measurements involve using the DVM to insure that the appropriate power is being applied to the proper pins of the RC5035 or RC5036.

1. **Check Power Supply.** Using the DVM, check that the VCCA pin (pin 6) has +5V.

2. **Check VREF Test Point.** Using the DVM, measure the voltage on the VREF pin (pin 2). This voltage should be 1.5V ±1%.

3. **Check Switch Control**. Using the DVM, measure the voltage on the SWCTRL pin (pin 16). A high level (+5V) on this pin will cause the switcher output of the RC5036 to be at +3.5V. (This is a no connect pin on the RC5035.)

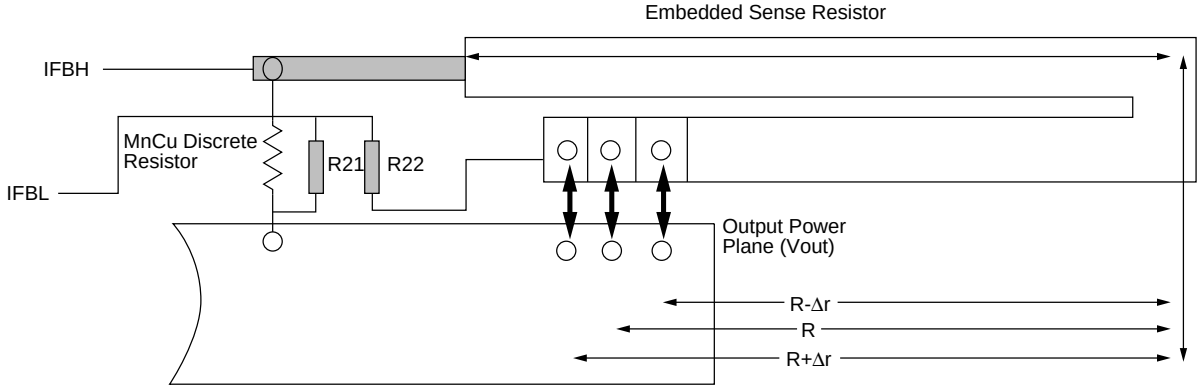


Figure 16. RC5036 Demo Board Sense Resistor Implementations

4. **Check VCCP**. Using the DVM, measure the VCCP pin (pin 10). This pin should be approximately 12V.

5. **Check VCCL**. Using the DVM, measure the VCCL pin (pin 11). This pin should also be approximately 12V.

6. **Check LIN_EN.** Using the DVM, measure the linear regulator enable pin 1. For the RC5036, a high level (+5V) on this pin enables the linear regulator operational amplifier. (This pin is a no connect on the RC5035).

7. **Check VSCL.** Using the DVM, measure the voltage on pin 13. This pin should measure very close to +5V for a no load condition on the linear regulator. A voltage difference between the VCC supply and VSCL of more than 50mV indicates a possible short circuit condition at the output of the linear regulator.

8. **Check the Linear Regulator Output.** Using the DVM, measure the output voltage of the linear regulator. For the appropriate feedback resistors, the output voltage should be 3.3V ±3%.

9. **Check C_{EXT}**. Using the oscilloscope, observe that there is a triangular wave shape on pin 15, see Figure 17. The frequency of this pin varies with the external capacitor selected and the output loading conditions.

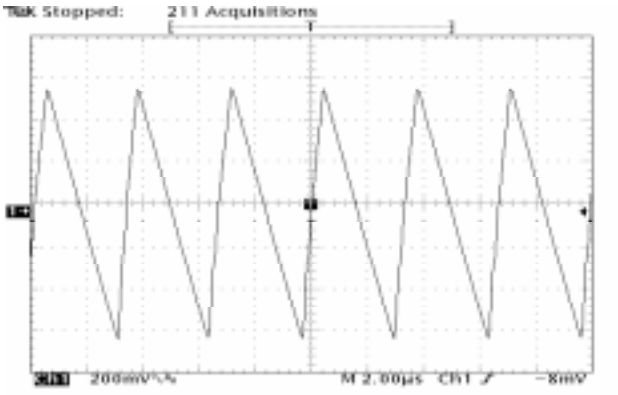


Figure 17. Timing Capacitor Waveform on Pin 15

10. **Check the Switcher Output Voltage.** Using the DVM, measure the voltage at the output of the switching regulator circuit after the sense resistor. For the RC5036, the output voltage should measure 3.5V ±3%. (The voltage output for the RC5035 and RC5036 and RC5036 with SWCTRL low depends on the external feedback resistor ratio). Using the active load connected to the output of the voltage regulator, apply a light loading condition, approximately 100mA, then measure the switcher output again. The voltage should remain at 3.5V.

If all of the above conditions check correctly, then proceed to the next step in the verification process. If you have any problems obtaining acceptable results from the above steps, then, most likely, one or more of the external parts is either connected incorrectly or is faulty.

Step 2: Verification

1. **Load Regulation Check.** This step involves using the active current load to check the load regulation of the supply through its specified load range. The active load should be connected to the output of the switching supply and the DVM, as is used to measure the supply output voltage at the CPU socket. First, set the active load to 0.5A, then measure Vout. Increase the active load to 1A, then 2A, and so on through the specified load range. Each time record the output voltage. The load regulation is then calculated by the following equation:

$$LR = \frac{V_{OUT}(I_{MAX}) - V_{OUT}(I_{MIN})}{V_{OUT}(IDEAL)} \times 100 = \%$$

   Both, the switching supply and the linear regulator should be checked for load regulation throughout the current specified range.

2. **Efficiency.** The efficiency of the switching regulator can also be measured and compared to the calculated value to determine if the selected components are operating within their specified ranges. Excessive efficiency losses indicate that one or more components are being stressed beyond their specified temperature limits. The efficiency of a switching power supply is simply calculated from the following relationship:

$$EFF = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100 = \%$$

   This efficiency number can be compared to the efficiency calculated from the estimations of the various losses in the components. The relationship is given as follows:

$$EFF = \frac{P_{OUT}}{P_{OUT} + PD_{TOTAL}} \times 100$$

   Where PD_{TOTAL} is the sum of all of the power losses in the circuit.

- MOSFET loss: $PD_{FET} = I^2 \times R_{DS(ON)} \times DutyCycle$
- Diode loss: $P_{DIODE} = I \times V_F \times (1-DutyCycle)$
- Inductor loss: $PIND = I^2 \times R_{DC}$
- Sense Resistor loss: $P_{RSENSE} = I^2 \times R$
- Gate Drive loss: $PGATE = Q_G \times f \times V_{GS}$
- IC power loss: $P_{IC} = V_{CC} \times I_{CC}$

*At the writing of this document, Intel has not made available a P55C tester. However, testers are available for P54 and P6; thus, a similar offering may be forthcoming for the P55C.

Step 3: Transient Response Test

This test evaluates the time taken for the regulator feedback loop to react to a step change in the output load current and then return to a specified steady-state voltage. This test is a measure of the regulator's ability to respond to a worst case change in current that might be demanded from the CPU (that is, sleep-to-full load). Several transient testers are available from Intel for the P54. These test boards fit directly onto the CPU socket and involve a scope measurement similar to the one shown below. Contact Intel for information on Transient Testers. (See Figure 18).

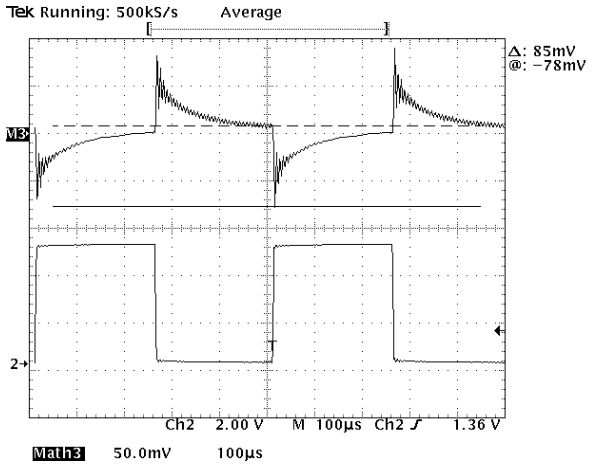


Figure 18. Transient Response of RC5036 Evaluation Board (0.5A to 5A Load Step)

Appendix A: Directory of Suppliers for Components

Dale Electronics, Inc.
E. Hwy. 50, PO Box 180
Yankton, SD 57078-0180
PH: (605) 665-9301

Fuji Electric
Collmer Semiconductor Inc.
14368 Proton Rd.
Dallas, Texas 75244
PH: (214)233-1589

Intel Corp.
5200 NE Elam Young Pkwy.
Hillsboro, OR. 97123
PH: (800) 843-4481 Tech. Support
for Power Validator

International Rectifier
233 Kansas St.
El Segundo, CA 90245
PH: (310) 322-3331

IRC Inc.
PO Box 1860
Boone, NC 28607
PH: (704) 264-8861

Mallory
North American Capacitor Co.
7545 Rockville Rd.
Indianapolis, IN 46214
PH: (317) 273-0090

Motorola Semiconductors
PO Box 20912
Phoenix, Arizona 85036
PH:(602) 897-5056

Nihon Inter Electronics Corp.
Quantum Marketing Int'l, Inc.
12900 Rolling Oaks Rd.
Caliente, CA 93518
PH: (805) 867-2555

Pulse Engineering
12220 World Trade Drive
San Diego, CA 92128
PH: (619) 674-8100

Sanyo Energy USA
2001 Sanyo Avenue
San Diego, CA 92173
PH: (619) 661-6620

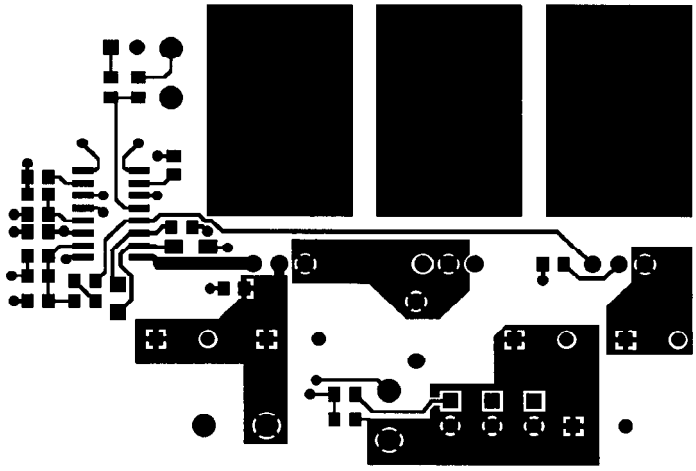
Sumida Electric USA
5999 New Wilke Road Suite #110
Rolling Meadows, IL 60008
PH: (708) 956-0702

Xicon Capacitors
PO Box 170537
Arlington, Texas 76003
PH:(800) 628-0544

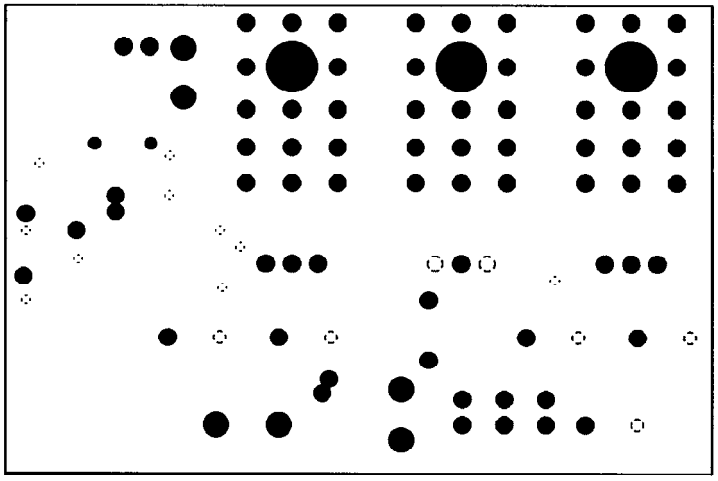
Appendix B: Bill of Materials and Gerber File

BOM for RC5036 Application circuits, Figures 5 and 6				
Quantity	**Reference**	**Manufacturer**	**Part Order #**	**Description**
4	C4,C5,C7,C14	Panasonic	ECU-V1H104ZFX	0.1µF 50V capacitor
1	C10	Panasonic	ECU-V1H153KBX	15nF capacitor
1	C6	Panasonic	ECU-V1H121JCG	180pF capacitor
1	C9	Panasonic	ECSH1CY105R	1µF 16V capacitor
4	C2,C3,C12,C13	Sanyo	6MV1500GX	1500µF 6.3V electrolytic capacitor 10mm x 20mm
1	C15	Sanyo	16MV330GX	330µF 16V electrolytic capacitor, 8mm x 15mm
1	DS1	Motorola	MBR1545CT	Schottky Diode, Motorola
1	L1	Pulse Engineering	PE-53682	4.7µH inductor
1	M1	Fuji	2SK1388	N-Channel Logic Level Enhancement Mode MOSFET
1	Q1	National	D44H11	NPN Power Transistor
1	R1	Copel	AWG #18	6 mΩ Iron Alloy resistor
1	R2	Panasonic	ERJ-6ENF1.74KV	1.74K 1% Resistor
1	R3	Panasonic	ERJ-6ENF2.00KV	2.00K 1% Resistor
1	R4	Panasonic	ERJ-6ENF12.1KV	12.1K, 1% Resistor
1	R5	Panasonic	ERJ-6ENF10.0KV	10K 1% resistor
1	R7	Panasonic	ERJ-6GEY100V	47Ω 5% resistor
1	R6	Copel	AWG #18	7 mΩ Iron Alloy resistor
1	U1	Raytheon	RC5036M	Dual Regulator for P55 - Switching regulator + Linear regulator

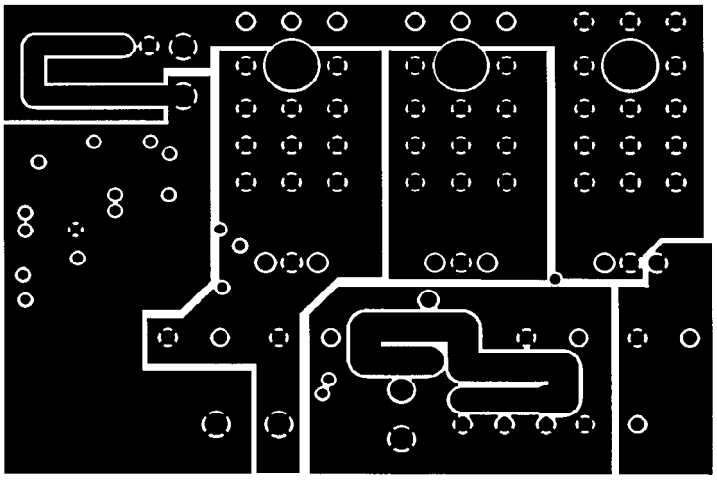
RC5036 Motherboard Layout Gerber File



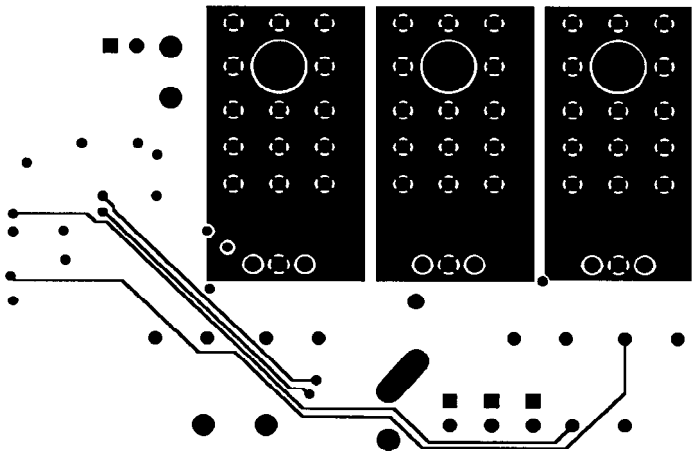
TOP



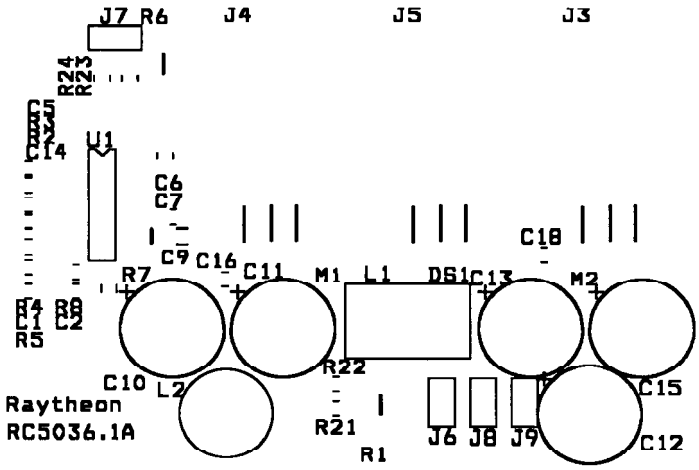
GND



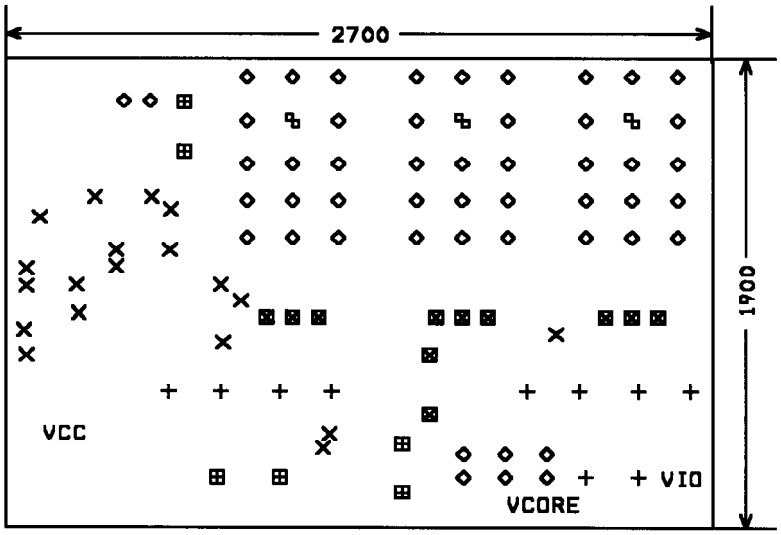
POWER



MOTTOB


J7 R6
J4
J5
J3
R24
R23
C5
C14
U1
C6
C7
C9
C16
C11
M1
L1
DS1
C13
M2
C18
R7
R4 R8
C1 C2
R5
C10
L2
R22
R21
R1
J6 J8 J9
C15
C12
Raytheon
RC5036.1A

TOP SILK


2700
1900
VCC
VIO
VCORE

Appendix C: Selected Component Specifications

Table 1. Power MOSFETS

MOSFET Selection Table

Manufacturer and Model #	Conditions (Note 1)		$R_{DS, ON}$ (mΩ) Typ.	$R_{DS, ON}$ (mΩ) Max.	Package	Thermal Resistance
Fuji 2SK1388	V_{GS} = 4V, I_D = 17.5A	T_J = 25°C	25	37	TO-220	Φ_{JA} = 75
		T_J = 125°C	37	—		
Siliconix SI4410DY	V_{GS} = 4.5V, I_D = 5A	T_J = 25°C	16.5	20	SO-8 (SMD)	Φ_{JA} = 50
		T_J =125°C	28	34		
National Semiconductor NDP706AL NDP706AEL	V_{GS} = 5V, I_D = 40A	T_J = 25°C	13	15	TO-220	Φ_{JA} = 62.5 Φ_{JC} = 1.5
		T_J = 125°C	20	24		
National Semiconductor NDP603AL	V_{GS} = 4.5V, I_D = 10A	T_J = 25°C	31	40	TO-220	Φ_{JA} = 62.5 Φ_{JC} = 2.5
		T_J = 125°C	42	54		
National Semiconductor NDP606AL	V_{GS} = 5V, I_D = 24A	T_J = 25°C	22	25	TO-220	Φ_{JA} = 62.5 Φ_{JC} = 1.5
		T_J = 125°C	33	40		
Motorola MTB75N03HDL	V_{GS} = 5V, I_D = 37.5A	T_J = 25°C	6	9	TO-263 (D^2 PAK)	Φ_{JA} = 62.5 Φ_{JC} = 1.0
		T_J = 125°C	9.3	14		
Int. Rectifier IRLZ44	V_{GS} = 5V, I_D = 31A	T_J = 25°C	—	28	TO-220	Φ_{JA} = 62.5 Φ_{JC} = 1.0
		T_J = 125°C	—	46		

Note:

1. $R_{DS, ON}$ values at T_J = 125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only. Only National Semiconductor offers maximum values at T_J = 125°C.

Table 2. Power Darlington Selection

Power Transistor Selection Table

Manufacturer and Model #	Conditions (Note 1)		β (h_{FE}) Typ.	β (h_{FE}) Min.	Package	Thermal Resistance
Various	Ic = 4A, Vce = 1V	T_J = 25°C	80	40	TO-220	Φ_{JA} = 75
D44HXX		T_J = 125°C		-		
Motorola	Ic = 3A, Vce = 2V	T_J = 25°C	80	40	TO-220	Φ_{JA} = 62.5
MJE15028						
		T_J = 25°C			TO-220	Φ_{JA} = 62.5
		T_J = 125°C				Φ_{JC} = 1.0

Table 3. Power Magnetics, Inductors

Device	Mfgr.	Parameter	Conditions	Max Value	Units
CDHR127-1R3NC	Sumida	DCR	25ºC	0.0101	Ω
PE-53680	Pulse Engr.	DCR	25ºC	0.004	Ω

Table 4. Capacitors

Device	Mfgr.	Parameter	Conditions	Max Value	Units
20SA100M	Sanyo	ESR	100-300kHz	0.037	Ω
6SA330M	Sanyo	ESR	100-300kHz	0.035	Ω
1000µF	XICON	ESR	100-300kHz	0.15	Ω
16MV330GX	Sanyo	ESR	10-200kHz	0.10	Ω
6MV1500GX	Sanyo	ESR	10-200kHz	0.044	Ω

Table 5. Schottky Diodes

Device	Mfgr.	Parameter	Conditions	Max Value	Units
C10T02QL	Nihon	Vf	If = 5A	0.47	V
MBRB1545CT	Motorola	Vf	If = 7.5A	0.57	V
MBRS140T3	Motorola	Vf	If = 1A	0.6	V
EC10QS02L	Nihon	Vf	If = 1A	0.45	V

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